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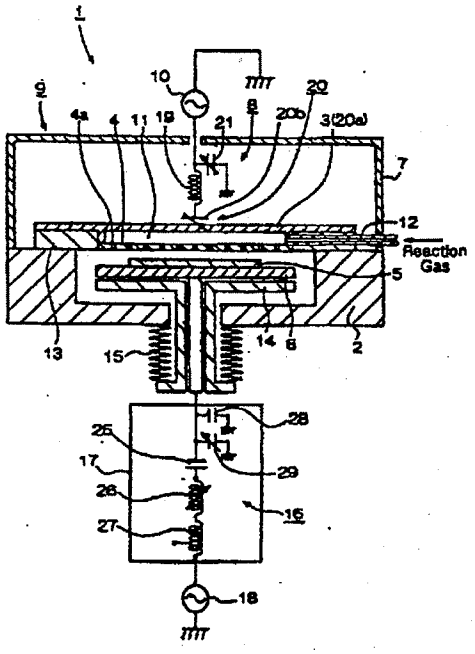
(54) Abstract Title
Forming silicon oxide layer by use of two frequency excitation plasma CVD

(57) A method of forming a silicon oxide layer comprises providing two frequency excitation plasma CVD device 1 which comprises a high frequency electrode 3, a susceptor electrode 6, and two matching boxes 8, 16 for impedance matching between the electrodes 3, 6 and power supplies 10, 18, wherein one side electrode constituting a tuning condenser 20 of a matching box 8 toward the high frequency electrode 3 is the high frequency electrode 3; placing a substrate 5 on the susceptor electrode 6; applying high frequency electric power on the high frequency electrode 3 and the susceptor electrode 6 respectively; and forming a silicon oxide layer on the substrate 5 by generating plasma with using a reaction gas of which main reaction gas is a mixing gas of monosilane and nitrous oxide.

FIG. 1



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DRAWINGS

FIG. 1

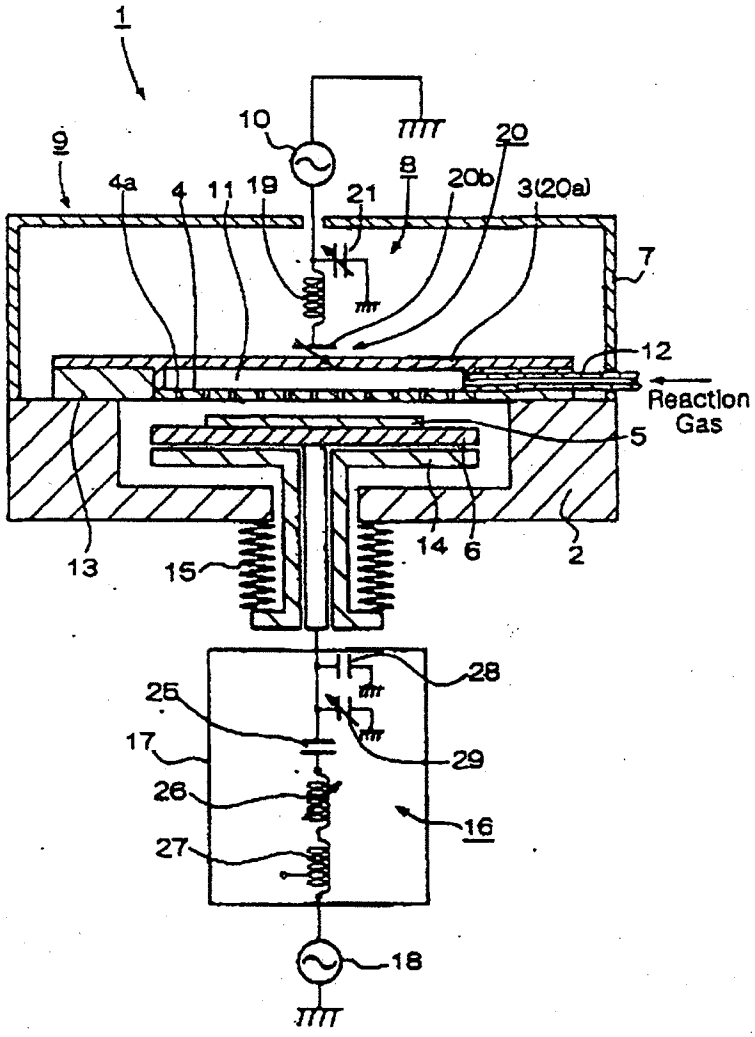


FIG. 2

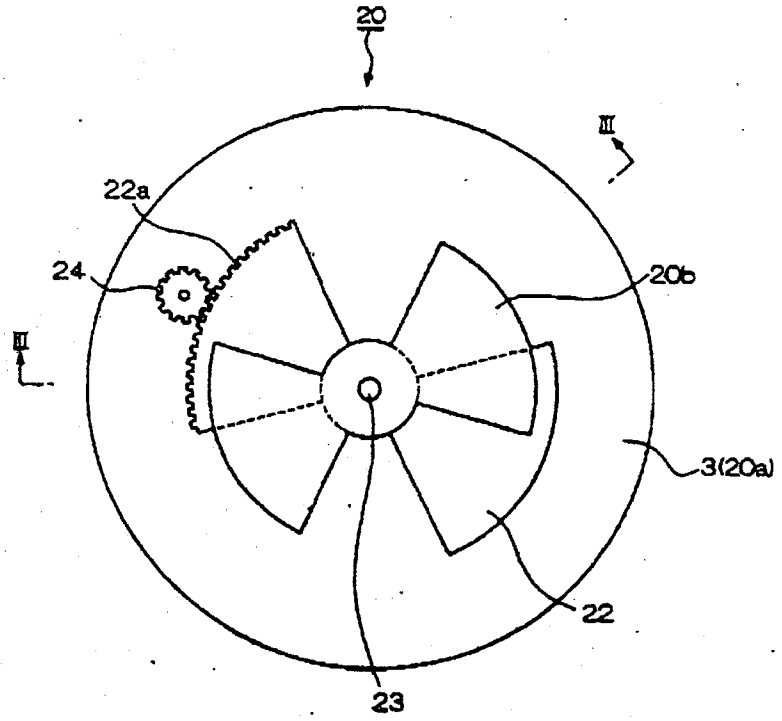


FIG. 3

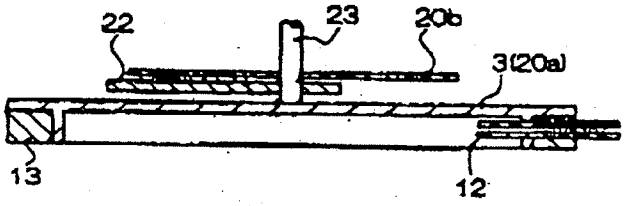


FIG. 4A

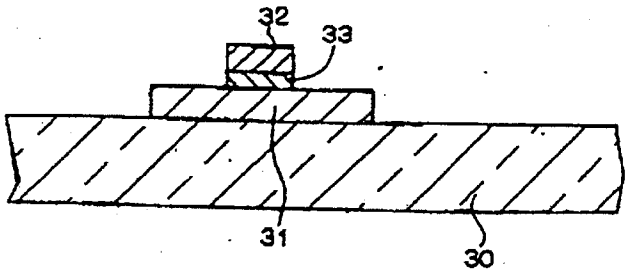


FIG. 4B

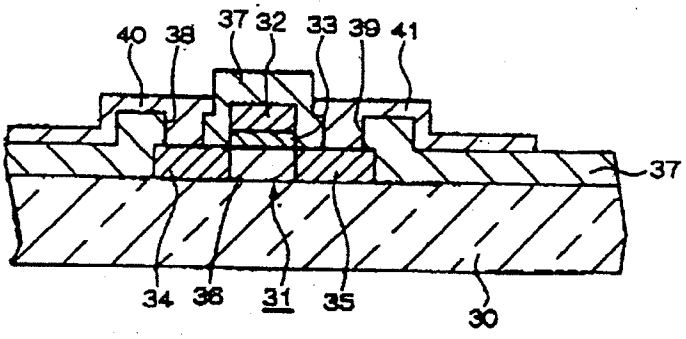


FIG. 4C

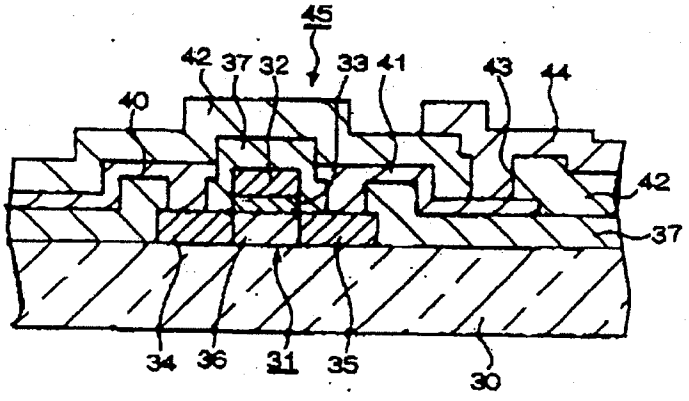


FIG. 5

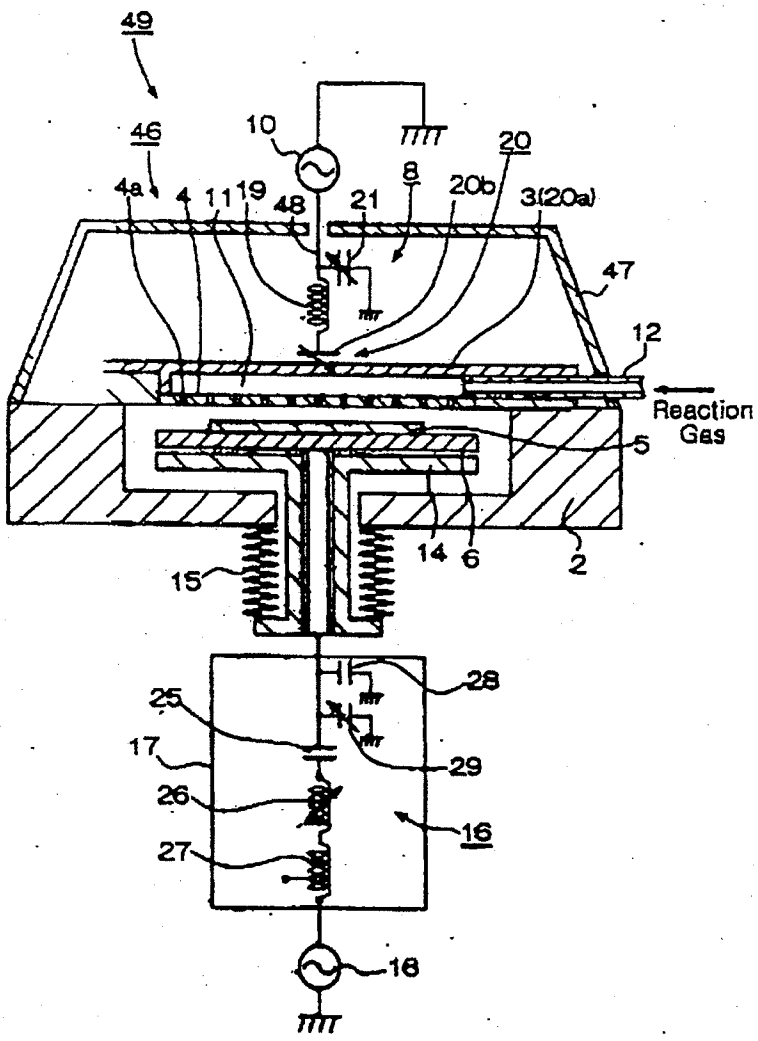

49
46
10
20
4a
4
11
19
48
21
8
20b
3(20a)
47
12
Reaction Gas
5
14
6
2
15
28
25
17
29
26
16
27
18

FIG. 6

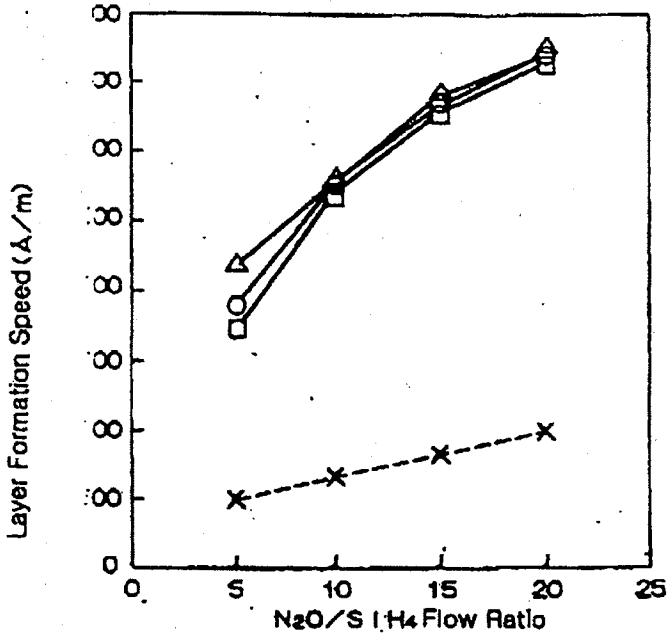

Layer Formation Speed (Å/m)
0
5
10
15
20
25
N2O/SiH4 Flow Ratio

FIG. 7

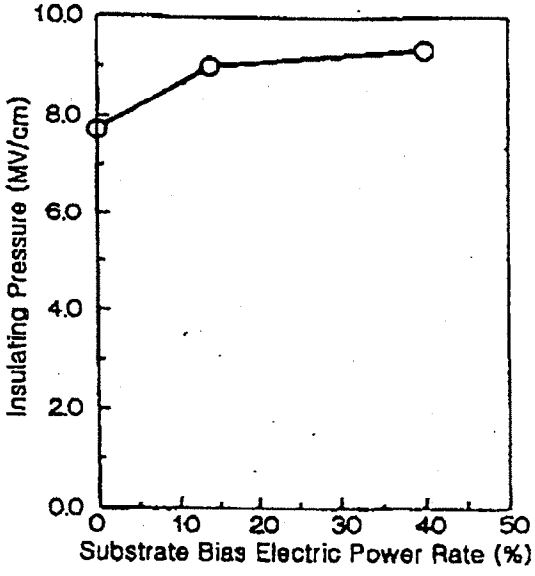

Insulating Pressure (MV/cm)
10.0
8.0
6.0
4.0
2.0
0.0
0
10
20
30
40
50
Substrate Bias Electric Power Rate (%)

FIG. 8

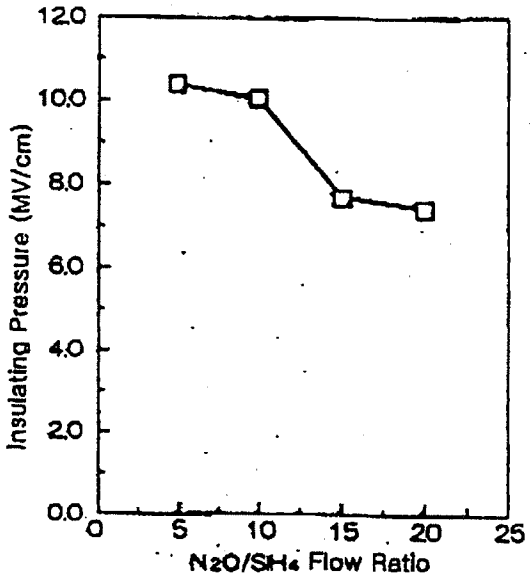

12.0
10.0
8.0
6.0
4.0
2.0
0.0
Insulating Pressure (MV/cm)
0
5
10
15
20
25
N2O/SiH4 Flow Ratio

FIG. 9

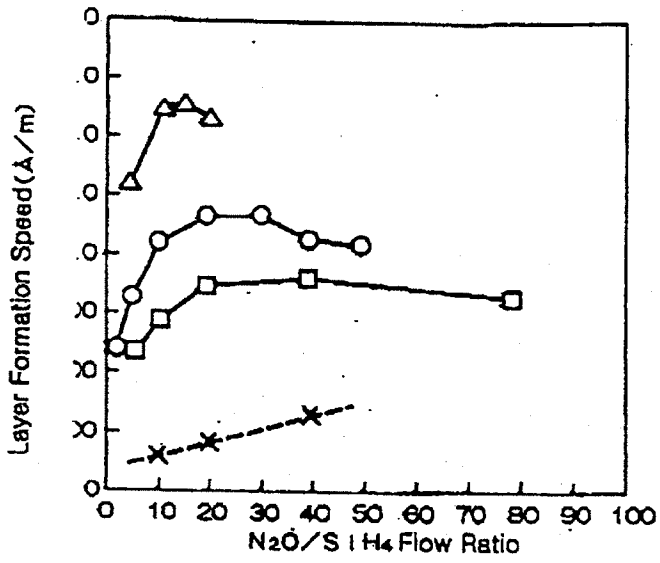

Layer Formation Speed (Å/m)
0
10
20
30
40
50
60
70
80
90
100
N2O/SiH4 Flow Ratio

FIG. 10

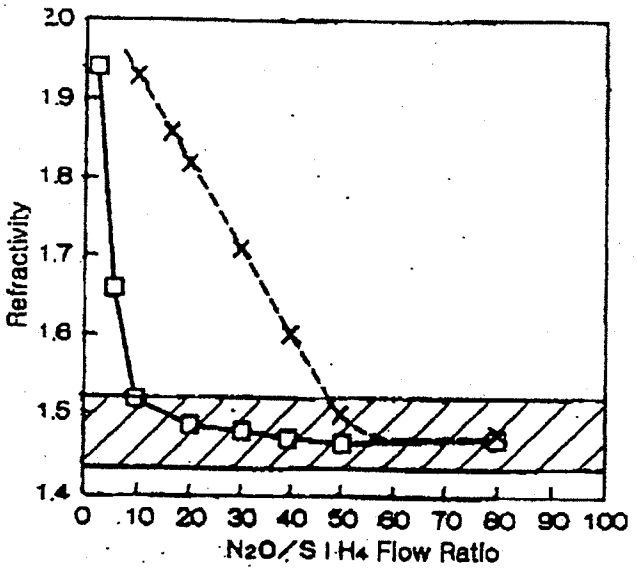

2.0
1.9
1.8
1.7
1.6
1.5
1.4
Refractivity
0 10 20 30 40 50 60 70 80 90 100
N2O/SiH4 Flow Ratio

FIG. 11

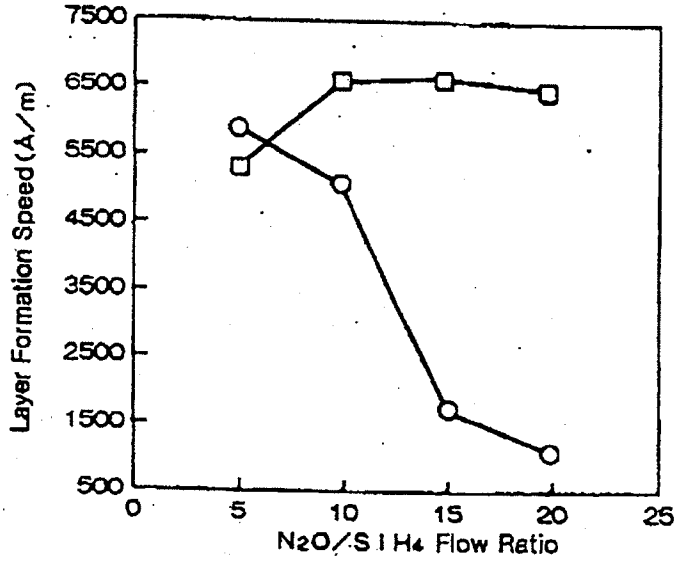

7500
6500
5500
4500
3500
2500
1500
500
Layer Formation Speed (Å/m)
0 5 10 15 20 25
N2O/SiH4 Flow Ratio

FIG. 12

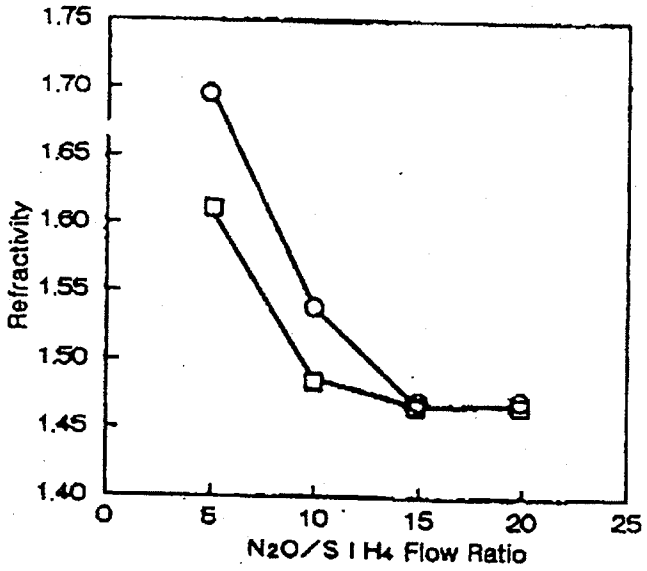
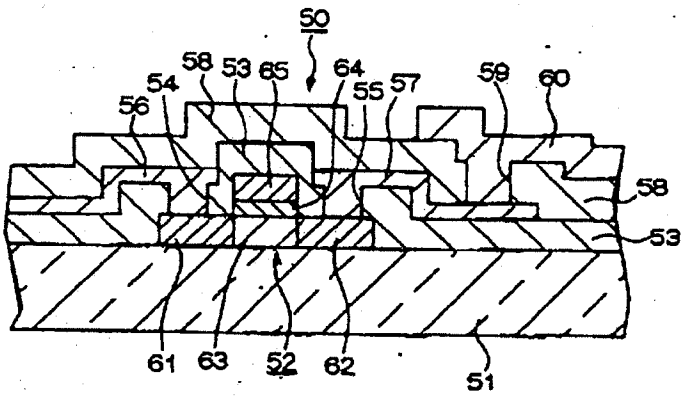


FIG. 13

PRIOR ART



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METHOD OF FORMING SILICON OXIDE LAYER AND METHOD OF MANUFACTURING THIN FILM TRANSISTOR THEREBY

The present invention relates to a method of forming silicon oxide layer and method of manufacturing thin film transistor (TFT) thereby, and more particularly, but not exclusively, to a method of forming silicon oxide layer preferably used as a gate insulator and an interspacing insulator.

A liquid crystal display device (LCD) has been used widely to be minimized, lightened and thinned, for example, an active matrix LCD of a twisted nematic (TN) mode has been known as a display device which has a low driving voltage, a small electric power consumption, a high contrast and a high image quality.

In the active matrix LCD, a pair of substrates oppose each other by interposing a liquid crystal layer, and one substrate between them is an active matrix substrate which has a switching element driving a pixel in each pixel.

Fig. 13 shows a TFT which is a switching element of the active matrix substrate, and more particularly shows a top-gate TFT. As shown in the figure, in the TFT 50, a semiconductive layer 52 is formed in an island type on a transparent substrate 51, and an interspacing insulator 53 is formed to cover the semiconductive layer 52 on the transparent substrate 51. In addition, contact holes 54, 55 are formed in the interspacing insulator 53, and source and drain electrodes 56, 57 are formed to connect the semiconductive layer 52 through the contact holes 54, 55 respectively.

Further, a passivation layer 58 is formed on the interspacing insulator 53 to cover the source and drain electrodes 56, 57, a contact hole 59 is formed in the passivation layer 58, and a pixel electrode 60 is formed to connect to the drain electrode 57 through the contact hole 59.

The semiconductive layer 52 comprises a source region 61, a drain region 62, and a channel region 63 between the source and drain regions 61, 62. The source electrode 56 is connected to the source region 61 and the drain electrode 57 is connected to the drain region 62. A gate insulator 64 is formed on the channel region 63 of the semiconductive layer 52, and a gate electrode 65 is formed on the gate insulator 64.

As to the TFT 50 shown in the Fig. 13, generally, the semiconductive layer 52 includes amorphous silicon (a-Si) or poly-silicon (Poly-Si), the source, drain and gate electrodes 56, 57, 65 include conductive metals, and the pixel electrode 60 is formed as a transparent conductive layer of Indium Tin Oxide (ITO).

The insulating layer such as the gate insulator 64, the interspacing insulator 53, and the like includes silicon oxide (SiO_2) layer. In the TFT 50, the electric charge induced on the channel region 63 is controlled by the electric field when a voltage is applied to the gate electrode 65, which makes the current flowing between the source and drain electrodes to be on or off. The TFT functions as a switching element.

As described above, while it is necessary an insulating layer such as the gate insulator, the interspacing insulator, and the like to the TFT, the capabilities required to the gate insulator and

interspacing insulator are different from each other respectively.

The gate insulator is the most important element which affects the electric characteristic of the TFT, for example a threshold voltage, and so on. Hence, as the material for the gate insulator, it is required that the characteristic is stable and the insulating pressure is good although the thickness of the insulating layer is thin.

On the other hand, the interspacing insulator maintains the insulation between the conductive layers by interposing between two different conductive layers as being between the gate and source electrodes, or between the gate and drain electrodes.

As shown in the Fig. 13, however, the interspacing insulator is formed according to the step of the gate electrode or semiconductive layer, so that if the step coverage of the interspacing insulator is bad, there is a problem that the insulating pressure at the steps is lowered. Therefore, it is required the interspacing insulator which has a good step coverage and particularly has a high insulating pressure at the steps.

To form the silicon oxide layer used in these insulating layers, it has been known to employ the plasma CVD using tetraethlyorthosilicate (TEOS) as the material gas. Since the silicon oxide layer of TEOS group has a good step coverage, it is suitable for the interspacing insulator. However, there are problems in that the formation speed of the layer is slow, the insulating pressure is low, and so on; further, it could not be used as the gate insulator. Moreover, TEOS is in a liquid state at room temperature, so that it is difficult to

employ the CVD using the TEOS after vaporizing this, and there is also the matter of high costs.

In addition, to form the silicon oxide layer used in these insulating layers, it has been known to employ a plasma CVD using the mixing gas of monosilane (SiH_4) and nitrous oxide (N_2O) as the material gas. Regarding this silicon oxide layer, because the step coverage is too bad and there is a concern of generating cracks from the steps into the layer; it could be used to the gate insulator, but it is not suitable for the interspacing insulator.

As described above, as to the insulating layer in the TFT, since the capabilities required according to the uses such as the gate insulator, the interspacing insulator, and the like differ respectively, it is necessary to use the material of the insulating layer according to the uses. However in this case, because of the process limitation according to the material gas, the degree of freedom in the process is lowered and it becomes a bad manufacturing process with a small productivity.

Therefore, although the silicon oxide layer is formed by the plasma CVD using same material gas, it could be used without regard to the uses such as the gate insulator, the interspacing insulator, and the like, and then it is required for rationalizing of the manufacturing process.

Accordingly, the present invention is directed to a method of forming silicon oxide layer that substantially obviates one or more problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method of forming a silicon oxide layer being used as a gate insulator and an interspacing insulator. The silicon oxide layer has good characteristics such as the insulating pressure or the step coverage, improving the yield of the TFT, having no problems of treatment or cost. Another object of the present invention is to provide a method of manufacturing a TFT using the silicon oxide layer.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve the objects and in accordance with the purpose of the invention, as embodied and broadly described herein, the method of forming a silicon oxide layer comprises the steps of:

providing two frequency excitation plasma CVD device which comprises a first high frequency power supply, a high frequency electrode connected to the a first high frequency power supply, a matching box toward the high frequency electrode having a matching circuit obtaining a matching of impedance between the first high frequency power supply and high frequency electrode; a second high frequency power supply, a susceptor electrode connected to the second high frequency power supply opposing the high frequency electrode and supporting a substrate, and a matching box toward the susceptor electrode having a

matching circuit obtaining a matching of impedance between the second high frequency power supply and susceptor electrode, wherein one electrode among at lease two electrodes which constitute at least tuning condenser in the matching circuit of the matching box toward the high frequency electrode is the high frequency electrode;

placing the substrate on the susceptor electrode;

applying high frequency electric power on the high frequency electrode and the susceptor electrode respectively; and

forming a silicon oxide layer on the substrate by generating plasma with using a reaction gas in which a flow ratio of the mixing gas of monosilane and nitrous oxide is 10 to 50%.

In the conventional plasma CVD device, a susceptor placing a substrate was provided in a chamber, an electrode was formed corresponding thereto, a high frequency electric power is applied to the electrode, and plasma was generated by leading a reaction gas.

As to the above constitution, the present inventors had already filed a Patent Application directed to a two frequency excitation plasma CVD device that where susceptor placing the substrate would be an electrode and then bias electric power could be applied to the substrate.

Among the two matching boxes between the first high frequency power supply and high frequency electrode, and the second high frequency power supply and susceptor electrode, if one side electrode of the tuning condenser in the matching circuit of the matching box toward the high frequency electrode is used as the high frequency electrode, it is possible to obtain a plasma CVD device

having the advantages that the electric power decreases, the electric power consumption efficiency is high, the layer formation speed is rapid, and then it could obtain the layer with a good quality.

Therefore, the present inventors use the two frequency excitation plasma CVD device with the matching box, the material gas of which main reaction gases are monosilane gas and nitrous oxide gas widely used in forming a silicon oxide layer. And the formation of the silicon oxide layer is performed with changing the formation condition such as the flow ratio of gases, etc.

As the result, in the two frequency excitation plasma CVD device, if it use the reaction gas in which the flow ratio of the mixing gas of monosilane and nitrous oxide is 10 to 50%, it could obtain the silicon oxide layer as good as the silicon oxide layer of the TEOS group, although the N_2O/SiH_4 based silicon oxide layer has bad step coverage compared with the conventional silicon oxide layer of the TEOS group.

As to the reaction gas, the flow ratio of nitrous oxide to monosilane is preferably 10 or more.

If the flow ratio of nitrous oxide to monosilane is 10 or more, the stoichiometric structure of the silicon oxide layer is proved by the refractivity experiment and a silicon oxide layer having a sufficiently high formation speed is obtained. From the above, the step coverage is improved, and when the flow ratio is 10 or more, the insulating pressure is enhanced, also.

As to the reaction gas of which main gases are 10 to 50% of nitrous oxide and monosilane, other gas among the reaction gas includes a gas selected from the group

consisting of helium, hydrogen, xenon, oxygen, argon, nitrogen and a mixture thereof.

These gases affect secondarily to the reaction of the main reaction gas. For example, helium, hydrogen and xenon accelerate the reaction at the point that ionization energy is high, and have an effect of improving the stability of the plasma. Oxygen supplies the quantity of oxygen ion on the formation of the layer. Argon and nitrogen accelerate the kinetic energy of the various ions generated by the main reaction gas, and then accelerate the reaction.

As to the two frequency excitation plasma CVD device, the frequency of the high frequency electric power applied to the high frequency electrode is in range of 13.56MHz to 100MHz. If the frequency of high frequency electric power applied to the high frequency electrode is below 13.56MHz, the potential difference between the high frequency electrode and the excited plasma is higher, the high frequency electrode is easily damaged and then it is not practical.

Further, when the frequency of high frequency electric power applied to the high frequency electrode is over 100MHz, the manufacturing of the power supply is difficult, and the output is unstable, and then it is not practical.

On the other hand, if a frequency of high frequency electric power applied to the susceptor electrode is below 50kHz, the susceptor electrode is easily damaged like the high frequency electrode. If the frequency is over 1.6MHz, it is difficult to discharge between the high frequency electrode the susceptor electrode, the

electric power consumption efficiency decreased, and then it is not practical.

The present embodiments provide the silicon oxide layer having a high formation speed of the layer and a good quality. However, in the matching box toward the high frequency electrode of the two frequency excitation plasma CVD device, a feed wire providing the high frequency electrode with the high frequency electric power in the first high frequency supply through the matching circuit is not parallel with a side wall of a housing having a conductive material in the matching box.

In the two frequency excitation plasma CVD device, the high frequency current on supplying power flows through the high frequency power supply, coaxial cable, matching circuit, feed wire, high frequency electrode, plasma space, susceptor electrode, side wall of chamber, and housing side wall of matching box.

However, if the side wall of the housing is not parallel with the feed wire, the flowing directions of the going and returning currents are not parallel with each other, and it prevents the mutual inductance from increasing. Therefore, the electric power consumption efficiency increases, and it improves the formation speed of the layer and the quality of the layer.

The present method of manufacturing a thin film transistor comprises forming a gate insulator and an interspacing insulator of the thin film transistor with the silicon oxide layer obtained by the method of forming the silicon oxide layer as described above.

From the method of forming the silicon oxide layer, it improves the electric power consumption efficiency of the plasma CVD device and the formation speed of the

layer. Further, the formation speed of the layer on a small substrate increases by applying the bias electric power on the substrate, and then the step coverage becomes preferable.

Hence, the N_2O/SiH_4 based silicon oxide layer is able to be used as the interspacing insulator as the conventional TEOS based silicon oxide layer is. Furthermore, since the improvement of the layer quality, particularly, the improvement of the insulating pressure is obtained, it is possible to apply to the gate insulator.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

For a better understanding of the present invention, embodiments will now be described by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a schematic sectional view showing two frequency excitation plasma CVD device used in forming a silicon oxide layer according to an embodiment of the present invention.

Fig. 2 is a plan view of the tuning condenser in the matching box toward the high frequency electrode of the Fig. 1.

Fig. 3 is a sectional view taken along the line III-III of the Fig. 2.

Fig. 4 is a manufacturing processing view showing the method of manufacturing a TFT using the method of a silicon oxide layer of the present embodiment.

Fig. 5 is a sectional view showing other example of two frequency excitation plasma CVD device used in the method of Fig. 4.

Fig. 6 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the formation speed in variation of the substrate bias electric power rate, which represents the results from the first embodiment of the present invention.

Fig. 7 is a graph showing the relation of the substrate bias electric power rate versus the insulating pressure of the silicon oxide layer, which represents the results from the second embodiment of the present invention.

Fig. 8 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the insulating pressure of the silicon oxide layer when the substrate bias electric power rate is not applied, which represents the results from the second embodiment of Fig. 7.

Fig. 9 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the formation speed of the silicon oxide layer in variation of SiH_4 flow ratio occupied in the reaction gas, which represents the results from the third embodiment of the present invention.

Fig. 10 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the refractivity of the silicon oxide layer, which represents the results from the third embodiment of Fig. 9.

Fig. 11 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the formation speed of the silicon oxide layer in each case of adding and non-adding He gas into the main reaction gas, which represents the results from the fourth embodiment of the present invention.

Fig. 12 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the refractivity of the silicon oxide layer in each case of adding and non-adding He gas into the main reaction gas, which represents the results from the fourth embodiment of Fig. 11.

Fig. 13 is a sectional view showing a conventional top-gate TFT.

Hereinafter, the embodiments of the present invention are explained in detail by accompanying the drawings.

Fig. 1 is a schematic sectional view showing two frequency excitation plasma CVD device 1 used in forming a silicon oxide layer according to an embodiment of the present invention.

The two frequency excitation plasma CVD device 1 comprises a high frequency electrode placed on a chamber and a susceptor electrode supporting a substrate, and applies high frequency electric power on both of the high frequency electrode and the susceptor electrode.

As shown in the Fig. 1, a high frequency electrode 3 and a shear plate 4 are mounted on a chamber 2, and a susceptor electrode 6 placing a substrate 5 is mounted corresponding to the shear plate 4 below the chamber 2. The high frequency electrode 3 is connected to a first high frequency power supply 10 by interposing a matching box toward the high frequency electrode 9 storing a matching circuit 8 in a housing 7 including conductive material.

Also, a space 11 is formed between the high frequency electrode 3 and the shear plate 4, and a gas leading pipe 12 is mounted to lead a reaction gas into the space 11. The reaction gas entered into the space 11

through the gas leading pipe 12 is provided in the chamber 2 from a plurality of holes 4a of the shear plate 4. The reference number 13 represents an insulator for insulating the high frequency electrode 3 from the wall part of the chamber 2.

A susceptor seal 14 is mounted around the susceptor electrode 6 and the susceptor electrode 6 and the susceptor seal 14 are constituted to move upward and downward by a bellows 15. From the above construction, the distance between the high frequency electrode 3 and susceptor electrode 6 could be controlled. Further, the susceptor electrode 6 is connected to a second high frequency electric power supply 18 by interposing the matching box toward the susceptor electrode 17 storing the matching circuit 16 therein.

In the matching box toward the high frequency electrode 9, the matching circuit 8 is mounted to match the impedance between the first high frequency power supply 10 and high frequency electrode 3 in the housing 7. The matching box toward the high frequency electrode 9 is a specific feature of the present embodiments. The detailed constitution of the matching circuit 8 is that a coil 19 and a tuning condenser 20 are connected in series to the first high frequency power supply 10, and a road condenser 21 is connected in parallel thereto and the end thereof is grounded. Between the two electrodes 20a, 20b of the tuning condenser 20, one electrode 20a is the high frequency electrode 3.

In this matching circuit 8, the impedance between the first high frequency power supply 10 and the high frequency electrode 3 is adjusted by controlling the capacity of the tuning condenser 20.

Figs. 2 and 3 are views of the tuning condenser 20 and this tuning condenser 20 is a butterfly type condenser. On the high frequency electrode 3 (also used as an electrode 20a of the tuning condenser), an insulation plate 22 having a north of a fan shape is supported to rotate on a shaft 23, and an electrode 20b is fixed to the shaft 23 to place the insulation plate 22 therebetween (the electrode 20b and the high frequency electrode 3).

In addition, from rotating the insulation plate 22 with using groove 22a and gear 24 formed thereon, the overlapped area between the electrode 20b and insulation plate 22 is changed, and then the tuning is performed the capacity between the electrodes 20a and 20b to be in a needed value.

On the other hand as shown in the Fig. 1, in the matching box 17 toward the susceptor electrode, the matching circuit 16 is mounted to match the impedance between the second high frequency power supply 18 and the susceptor electrode 6. The matching box 17 toward the susceptor electrode is a conventional type.

In the matching circuit 16, the tuning coils 26, 27 are connected in series to one side electrode of the condenser 25, and two road condensers 28, 29 are connected to the other side electrode of the condenser 25, the other ends of the road condensers are grounded.

To forming a silicon oxide layer with using the above plasma CVD device 1, the substrate 5 is placed on the susceptor electrode 6, and the high frequency electric power is applied to the high frequency electrode 3 and the susceptor electrode 6 from the first and second high frequency power supplies 10, 18. The silicon oxide

layer is formed on the substrate 5 by providing a reaction gas in the chamber 2 through the shear plate 4 in the gas leading pipe 12 and generating plasma.

As the reaction gas, the main reaction gases are monosilane and nitrous oxide and it further includes any other gases, and the flow ratio of the main reaction gas is 10 to 50%. The other gases include a gas selected from the group consisting of helium, hydrogen, xenon, oxygen, argon, nitrogen and a mixture thereof.

As to the main reaction gas, for example nitrous oxide 400sccm to 40sccm monosilane, it is preferable that the flow ratio of nitrous oxide to monosilane is 10 or more. From the above, the formed layer is surely the silicon oxide layer with sufficiently high formation speed of the layer.

The formation condition of the layer is, for example, 300°C of temperature, 200Pa of pressure, 10 of the flow ratio of nitrous oxide to monosilane, 35% (dilution with He) of the flow ratio of the mixing gas of nitrous oxide and monosilane occupied in the reaction gas, 13.56MHz to 100MHz of the frequency of the high frequency electric power applied to the high frequency electrode, 50kHz to 1.6MHz of the frequency of the substrate bias electric power applied to the susceptor electrode, and 40% of the ratio of the high frequency electric power applied to the susceptor electrode to the sum of the high frequency electric power applied to the high frequency electrode and the high frequency electric power applied to the susceptor electrode (hereinafter, it is referred to a substrate bias electric power rate).

Consequently, Fig. 4 is a manufacturing processing view showing the method of manufacturing a top-gate TFT

using the silicon oxide layer as a gate insulator and interspacing insulator.

As shown in the Fig. 4A, a semiconductive layer 31 of amorphous silicon in 500Å of the thickness is formed on a transparent substrate 30 such as a glass, and the semiconductive layer 31 is patterned in an island shape by a photolithography process. A silicon oxide layer is formed of 300Å the thickness over the whole surface.

At this time, the two frequency excitation plasma CVD device 1 and a reaction gas of which main reaction gases are nitrous oxide to monosilane are used. Further, after forming a metal layer of Al and the like of 1000Å of the thickness whole over the surface, the metal layer and the silicon oxide layer are patterned by the photolithography process, and the result thereof, the gate electrode 32 and the gate insulator 33 are formed.

As shown in the Fig. 4B, a region except the lower side of the gate electrode 32 among the semiconductive layer 31 is made an n-type silicon layer by ion-doping impurities such as phosphorus, arsenic and so on into the upper side of the gate electrode 32, and is formed a source region 34 and a drain region 35. At this time, the region between the source and drain regions 34, 35 is a channel region 36.

An interspacing insulator 37 of silicon oxide layer of 2000Å the thickness is formed all over the surface. At this time, it use the two frequency excitation plasma CVD device 1 and a reaction gas of which main reaction gases are nitrous oxide to monosilane are used.

The interspacing insulator 37 is patterned by photolithography process, and contact holes 38, 39 are formed to reach the source, drain regions 34, 35 of the

semiconductive layer 31, respectively. A metal layer of Al, etc. of 1000Å the thickness is formed all over the surface and patterned to form the source electrode 40 and the drain electrode 41, respectively.

As shown in the Fig. 4C, a passivation layer 42 of silicon nitride layer is formed all over the surface, patterned by photolithography process, and then a contact hole 43 is formed to reach the drain electrode 41. In addition, a transparent conductive layer of ITO, etc. is formed all over the surface and patterned to be a pixel electrode 44. From the above processes, a TFT 45 connecting the pixel electrode 44 is completed.

From the method of forming a silicon oxide layer of the present embodiments, since it use two frequency excitation plasma CVD device and one side electrode 20a of the tuning condenser 20 of the matching box toward the high frequency electrode 9 is used as the high frequency electrode 3 also, the electric power loss of the applied high frequency electric power heavily decreases as compared with the prior art. As the result, the electric power consumption efficiency increases, and it is possible to obtain the silicon oxide layer with high quality and high formation speed.

Therefore, in the method of manufacturing the TFT with the silicon oxide layer according to the present embodiments, although it may use N_2O/SiH_4 based silicon oxide layer as the interspacing layer 37, a good step coverage could be obtained as compared with the prior TEOS based silicon oxide layer. Also, since the insulating pressure is sufficiently high, it could be obtained the gate insulator 33 with a high reliability by N_2O/SiH_4 based silicon oxide layer.

Moreover, the present method could use the reaction gas of which main gases are nitrous oxide to monosilane that are very widely used; thus it is possible to complete without using the conventional TEOS gas. Hence, there are not the problems that the handling of the gas is difficult and the costs are high, and the yield and productivity of the TFT increase.

Furthermore, it will be apparent to those skilled in the art that various modifications can be made in the present invention without departing from the sprit or scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

For example, the formation condition of the layer of the CVD, etc. in the above embodiments may be only an example, it is possible to differ therefrom. In addition, the present method of manufacturing TFT is applied the top-gate TFT; however, it could apply to a bottom-gate TFT.

The plasma CVD device 1 used in the formation of the layer in the Fig. 1 has the side wall of the housing 7 in the matching box toward the high frequency electrode 9 being parallel with the feed wire. As shown in the Fig. 5, however, it is possible to use the side wall of the housing 47 in the matching box toward the high frequency electrode 46 not being parallel with the feed wire 48.

In this plasma CVD device 49, on feeding an electric power, the flowing directions of the going and returning currents of the high frequency current are not parallel with each other, and this prevents the mutual inductance from increasing. As the result, it improves the electric

power consumption efficiency, the formation speed of the silicon oxide layer, and the quality of the layer.

As to the Fig. 5, the same numeric references are applied to the same constituents in the Fig. 1.

EMBODIMENTS

Embodiment 1

The present embodiment formed the silicon oxide layer by using the two frequency excitation plasma CVD device with the matching box described above.

Fig. 6 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the formation speed in variation of the substrate bias electric power rate(rf_2) applied to the susceptor electrode when it used the two frequency excitation plasma CVD device of the above embodiment. The horizontal axis represents N_2O/SiH_4 flow ratio, and the vertical axis represents the formation speed.

The formation condition of the layer was that the frequency of the high frequency electric power applied to the high frequency electrode was 13.56MHz, the electric power (rf_1) was fixed, the frequency of the substrate bias electric power applied to the susceptor electrode was 1.6MHz, and the substrate bias electric power rate was 33.3% (this was represented as □ and solid line in the Fig. 6), 50% (this was represented as O and solid line in the Fig. 6), and 66.6% (this was represented as Δ and solid line in the Fig. 6). The temperature of the substrate was 300°C, the pressure in the chamber is 200Pa.

The comparative example was performing the same formation of the layer with using the conventional device having only the high frequency electrode that the high

frequency electric power of the 13.56MHz frequency was applied to (this was represented as × and dotted line in the Fig. 6).

As shown in the Fig. 6, in case of the comparative example, the formation speed of the layer was only 1000Å/min or less when N_2O/SiH_4 flow ratio was in range of 5 to 20. On the other hand, in case of the present embodiment, when the substrate bias electric power rate was 33.3%, 50%, 66.6%, the layer formation speed was 2000Å/min and less or more on the N_2O/SiH_4 flow ratio of 5, and 3700Å/min and less or more on the N_2O/SiH_4 flow ratio of 20.

Hence, the present two frequency excitation plasma CVD device improved remarkably the layer formation speed as compared with the conventional device. In addition, in case of the present two frequency excitation plasma CVD device, when N_2O/SiH_4 flow ratio was higher, the formation speed of the layer was improved, and when the substrate bias electric power was higher, the formation speed of the layer was improved.

Embodiment 2

The variation of the insulating pressure of the formed silicon oxide layer was investigated according to the applied of the substrate bias electric power.

Fig. 7 is a graph showing the relation of the substrate bias electric power rate versus the insulating pressure of the silicon oxide layer with using the present two frequency excitation plasma CVD device. The horizontal axis represents the substrate bias electric power rate (%), and the vertical axis represents the insulating pressure(MV/cm).

The formation condition of the layer was that the frequency of the high frequency electric power applied to the high frequency electrode was 40.68MHz, the high frequency electric power rf_2 was fixed, the frequency of the substrate bias electric power applied to the susceptor electrode was 1.6MHz, the substrate bias electric power rate was 0%, 14.3%, 40%. The temperature of the substrate was 300°C, the pressure in the chamber is 200Pa.

As to the reaction gas, the N_2O/SiH_4 flow ratio was 15, the flow ratio of the mixing gas of monosilane and nitrous oxide occupied in the reaction gas was 46% (dilution with He), and the layer thickness of the silicon oxide layer was 2000Å.

Fig. 8 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the insulating pressure of the silicon oxide layer when the substrate bias electric power rate is not applied to the susceptor electrode (rf_2=0W). The horizontal axis represents the N_2O/SiH_4 flow ratio, and the vertical axis represents the insulating pressure MV/cm.

The formation condition of the layer was that the frequency of the high frequency electric power applied to the high frequency electrode was 13.56MHz, the electric power rf_1 was fixed. And, the temperature of the substrate was 300°C, the pressure in the chamber is 200Pa.

As to the reaction gas, the N_2O flow ratio was changed after the SiH_4/He flow ratio was fixed 5%, and the thickness of the silicon oxide layer was 2000Å.

When it did not apply the substrate bias electric power, as shown in the Fig. 8, the insulating pressure

was 10MV/cm or more in range of 5 to 10 of the N_2O/SiH_4 flow ratio, however, the insulating pressure decreased to 7 to 8MV/cm in 15, 20 of the N_2O/SiH_4 flow ratio. As shown in the Fig. 7, when the insulating pressure was 7.7MV/cm in 15 of the N_2O/SiH_4 flow ratio, the insulating pressure increased to approximately 9 MV/cm according to applying the substrate bias electric power rate in 14.3%, 40%. Hence, it proved the effect of improving the insulating pressure of the silicon oxide layer by applying the substrate bias electric power.

Embodiment 3

In the present method of forming the silicon oxide layer, the changes of the characteristics of the formed silicon oxide layer were investigated according to the variation of the N_2O/SiH_4 flow ratio.

Fig. 9 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the formation speed of the silicon oxide layer with using the two frequency excitation plasma CVD device. At this time, SiH_4 flow ratio occupied in the reaction gas was 1% (this was represented as □ and solid line in the Fig. 9), 2% (this was represented as O and solid line in the Fig. 9), 3% (this was represented as Δ and solid line in the Fig. 9).

The horizontal axis represents the N_2O/SiH_4 flow ratio, and the vertical axis represents the formation speed of the layer Å/min in Fig.9.

The formation condition of the layer was that the frequency of the high frequency electric power applied to the high frequency electrode was 40.68MHz, the frequency of the substrate bias electric power was 1.6MHz, and the substrate bias electric power rate was 33.3%. And, the

temperature of the substrate was 300°C, the pressure in the chamber is 200Pa..

The comparative example was performing the same formation of the layer with using the conventional device having only the high frequency electrode that the high frequency electric power of the 13.56MHz frequency was applied to (this was represented as × and dotted line in the Fig. 9).

Fig. 10 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the refractivity of the silicon oxide layer. The horizontal axis represents the N_2O/SiH_4 flow ratio, and the vertical axis represents the refractivity in Fig.10.

The formation condition of the layer was that the frequency of the high frequency electric power applied to the high frequency electrode was 40.68MHz, the frequency of the substrate bias electric power was 1.6MHz, and the substrate bias electric power rate was 33.3%. And, the temperature of the substrate was 300°C, the pressure in the chamber is 200Pa (this was represented as □ and solid line in the Fig. 10).

The comparative example was performing the same formation of the layer with using the conventional device having only the high frequency electrode that the high frequency electric power of the 13.56MHz frequency was applied to (this was represented as × and dotted line in the Fig. 10).

As shown in the Fig. 9, in case of comparative example the formation speed of the layer was 500 to 1500 Å/min in range of 5 to 50 of the N_2O/SiH_4 flow ratio. However, in the present embodiment, when SiH_4 flow ratio occupied in the reaction gas was 1%, 2%, 3%, the

formation speed of the layer was so high as compared with the comparative example.

From the data of the present embodiment, when the SiH_4 flow ratio was larger, the formation speed of the layer was higher, and when the layer formation speed was 3000 Å/min and less or more on the SiH_4 flow ratio of 1%, it increases to 6000 Å/min on the SiH_4 flow ratio of 3%.

From the data on the SiH_4 flow ratio being constant, when the N_2O/SiH_4 flow ratio was in range of 0 to 10, the formation speed of the layer increased rapidly, and then when the N_2O/SiH_4 flow ratio was 10 or more, the formation speed of the layer was approximately constant.

From the above results, since the stability and management of the layer were so good, it was preferable that it used the present high frequency excitation plasma CVD device and the N_2O/SiH_4 flow ratio was 10 or more.

Furthermore, in case of the comparative example as shown in the Fig. 10, when the N_2O/SiH_4 flow ratio increased from 10 to 50, the refractivity gradually intended to decrease from 2, and when the N_2O/SiH_4 flow ratio was approximately 50, the refractivity was in range of 1.4 to 1.5. When the range which the refractivity represented by the solid line was 1.4 to 1.5 was the region that SiO_2 had the stoichiometric structure thereof, and the fact that the refractivity had the above value represented that the formed layer surely would be SiO_2.

In case of the present embodiment as compared with the above, when the N_2O/SiH_4 flow ratio was in range of 0 to 10, the refractivity rapidly decreased, and when the N_2O/SiH_4 flow ratio was 10, the refractivity was in range of 1.4 to 1.5 and maintained the value in this range.

From the above results, when it used the present two frequency excitation plasma CVD device and the N_2O/SiH_4 flow ratio was 10 or more, it would obtain the silicon oxide layer having stoichiometric structure.

Embodiment 4

In the present method of forming the silicon oxide layer, the effect of other gases added to the main reaction gas to the layer formation was investigated.

Fig. 11 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the formation speed of the silicon oxide layer in each case of adding (this was represented as □ and solid line in the Fig. 11) and non-adding (this was represented as O and solid line in the Fig. 11) He gas into the main reaction gas, N_2O/SiH_4 with using the present two frequency excitation plasma CVD device. In case of adding He gas, the flow was 800sccm. The horizontal axis represents the N_2O/SiH_4 flow ratio, and the vertical axis represents the formation speed of the layer Å/min.

The formation condition of the layer was that the frequency of the high frequency electric power applied to the high frequency electrode was 40.68MHz, the frequency of the substrate bias electric power was 1.6MHz, and the substrate bias electric power rate was 33.3%. And, the temperature of the substrate was 300°C, the pressure in the chamber is 200Pa.

Fig. 12 is a graph showing the relation of N_2O/SiH_4 flow ratio versus the refractivity of the silicon oxide layer in each case of adding (this was represented as □ and solid line in the Fig. 12) and non-adding (this was represented as O and solid line in the Fig. 12) He gas

into the main reaction gas N_2O/SiH_4. The horizontal axis represents the N_2O/SiH_4 flow ratio, and the vertical axis represents the refractivity.

The formation condition of the layer was that the frequency of the high frequency electric power applied to the high frequency electrode was 40.68MHz, the frequency of the substrate bias electric power was 1.6MHz, and the substrate bias electric power rate was 33.3%. And, the temperature of the substrate was 300°C, the pressure in the chamber is 200Pa.

As shown in the Fig. 11, in case of non-adding He gas, when the N_2O/SiH_4 flow ratio exceeded 10, the formation speed of the layer decreased rapidly. However, in case of adding He gas in 800sccm of flow, although the N_2O/SiH_4 flow ratio was changed, it was able to maintain stable the rapid formation of the present silicon oxide layer.

Further, as shown in the Fig. 12, in case of adding He gas as compared with the case of non-adding He gas, the change rate of the refractivity to the N_2O/SiH_4 flow ratio decreased, and when the N_2O/SiH_4 flow ratio was in more smaller range, the refractivity was in range of 1.4 to 1.5 (stoichiometric structure range). Hence, as to the composition of the silicon oxide layer, the stability of the case of adding He gas was more preferable.

As described above, from the results of the first to fourth embodiments, the improvement of the formation speed of the silicon oxide layer and the insulating pressure was proved by using the two frequency excitation plasma CVD device and by using the main reaction gas which N_2O/SiH_4 flow ratio being 10 over in added the other gas such as He, etc.

Further particularly, it could be obtained the silicon oxide layer preferably used as the interspacing insulator being required the step coverage and the gate insulator being required the reliability in the insulating pressure.

Consequently, from using the present two frequency excitation plasma CVD device having the matching box, the electric power consumption efficiency is improved, and the formation speed of the layer increases. The formation speed of the layer on a substrate increases by the effect of applying the substrate bias electric power, the step coverage thereof would be good.

Therefore, the N_2O/SiH_4 based silicon oxide layer is able to be used as the interspacing insulator as the conventional TEOS based silicon oxide layer is. Furthermore, since the improvement of the layer quality, particularly, the improvement of the insulating pressure is obtained, it is possible to apply to the gate insulator.

Consequently, the TFT with high reliability could be obtained accompanying a good yield without using the TEOS based silicon oxide layer having the problem of handling the material gas and of the costs.

Claims:

1. A method of forming a silicon oxide layer, the method including:

providing a two frequency excitation plasma CVD device, the device having a susceptor electrode and a high frequency electrode;

placing the substrate on the susceptor electrode;

applying a high frequency electric power on the high frequency electrode and the susceptor electrode respectively; and

forming a silicon oxide layer on the substrate by generating plasma with using a reaction gas in which a flow ratio of the mixing gas of monosilane and nitrous oxide is 10 to 50%.

2. The method according to claim 1, wherein the two frequency excitation plasma CVD device comprises:

a first high frequency power supply;

a high frequency electrode connected to the a first high frequency power supply;

a matching box toward the high frequency electrode having a matching circuit obtaining a matching of impedance between the first high frequency power supply and high frequency electrode;

a second high frequency power supply;

a susceptor electrode connected to the second high frequency power supply opposing the high frequency electrode and supporting a substrate; and

a matching box toward the susceptor electrode having a matching circuit obtaining a matching of impedance between the second high frequency power supply and

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Application No: GB 9925564.8 **Examiner:** Pete Beddoe
Claims searched: 1-9 **Date of search:** 4 February 2000

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): C7F (FHB, FHE, FHX); H1K (KJACX, KJAD)

Int Cl (Ed.7): C23C (16/40, 16/50); H01J 37/32; H01L 21/316

Other: Online: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
Y	EP 0874391 A2	(APPLIED) see esp col13 line 1 - col15 line 23 & figs	1 at least
Y	EP 0759481 A1	(NOVELLUS) see esp col4 line 56 - col9 line 12 & figs	1 at least
Y	EP 0738003 A2	(MATSUSHITA) see esp col8 line 21 - col9 line 15 & figs	1 at least
Y	EP 0686708 A1	(OHMI) see esp embodiment 1 & figs	1 at least
Y	EP 0678903 A1	(TOKYO) see esp col2 lines 54-58, col5 line 1 - col7 line 36 & figs	1 at least
Y	US 5736423	(ADVANCED) see esp col1 line 62 - col2 line 32 & figs	1 at least
Y	US 5698062	(TOKYO) see esp claim 1, col11 line 36 - col12 line 62 & figs	1 at least
Y	US 4937095	(SANYO) see esp col4 line 4 - col5 line 40 & figs	1 at least
Y	WPI Accession no 98-236540 & JP 10074749 A (APPLIED) see abstract		1 at least

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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Category	Identity of document and relevant passage	Relevant to claims
Y	WPI Accession no 90-197031 & JP 2129377 A (NEC) see abstract	1 at least

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